RLG

UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/775,836	02/02/2001	Richard Bisinella	CALLINAN 207-KFM	1154

7590 11/09/2004

Karl F. Milde, Jr., Esq.
MILDE, HOFFBERG & MACKLIN, LLP
Suite 460
10 Bank Street
White Plains, NY 10606

EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 11/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/775,836	BISINELLA, RICHARD	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 August 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, and 3-5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morton (patent No. 6,088,783) in view of Potash (patent No. 4,760,518).

2. Morton taught the invention substantially as claimed including a data processing ("DP") system comprising:

a) Plurality of circuit elements comprising arithmetic logic units (107,110,111,112,113), memory (108) and input/output unit circuits (114,115) (e.g., see fig. 1);

b) The plurality components interconnected on a grid (crossbar switch 109) wherein each of the plurality of components can be switched under program control to be connected to a predetermined selection of one or more of the plurality of components to route data through the grid for processing by the predetermined selection of one or more of the plurality of components (e.g., see col. 21, line 41-col. 22, line 55, and col. 28, lines 44-55).

3. Morton did not expressly detail (claim 1) registers interconnected by the grid. Potash however taught registers (32,34,36,38) connected to components comprising ALUs (30) via a grid (40) (fig. 1).

4. It would have been obvious to one of ordinary skill in the DP art to combine the teaching of Morton and Potash. Morton taught passing data between processor via memory with data transmitted over a grid (e.g., see col. 21, lines 41-65). One of ordinary skill would have been motivated to incorporate the Potash teachings of connecting the registers to the grid for access in order to improve the access to the

registers for transfer of data in that the access path would have been more direct and therefore have improved access (e.g., see fig. 1 and col. 5, line 51-col. 6, line 15 of Potash).

5. As per claim 3, Morton taught a grid connector and interconnection logic (702,705,707,710) (109) (e.g., see col. 21, line 41-col. 22, line 55, and col. 28, lines 44-55).

6. As per claim 4, Morton taught instruction decode (e.g., see col. 16, lines 35-65) and Potash taught a decoder that for interpreting the instruction set of the microprocessor into timed operations of the microprocessor and a grid connector which provided logic for interconnecting a predetermined one or more of the plurality of components with one or more of other components of the plurality of components on to the grid (e.g., see col. 31, line 20-col. 32, line 62).

7. As per the further limitations of claim 5, Potash taught a second grid (44) coupled to the elements connected the first grid (40)(e.g., see fig. 1).

8. The rejections are maintained as set forth in the last office action (and repeated above).

Response to Arguments

Applicant's arguments filed 8/12/04 have been fully considered but they are not persuasive.

In the remarks, the applicant in substance argues:

a) it would not have been obvious or even possible for a person skilled in the art to combine the teachings of Morton and Potash. The Examiner contends that it would have been obvious to combine the teachings and reasons therefore are included in the outstanding rejections.

b) The Morton and Potash references do not teach core data transferring grid to transfer data from any processor element (PE) to any other (PE). First of all invention disclosed by in the instant application comprises parallel buses arranged vertical directions and conductors arranged in horizontal directions where each vertical bus is connected to a register (in figure 1 and 2) and each horizontal conductor is connected to a respective system element comprising ALUs, internal memories external memories and instruction set memories. In figure 8 the orientation is reversed namely the memory units are connected to the horizontal conductors (with the addition of a standard unit) and the ALUs (along with memory unit and standard unit) are connected to vertical conductors). Figure 8 shows connection points where the horizontal and vertical conductors cross in the arrangement of an array. Figure 9 provides for connection between two of the combination of elements of figure 8. The Examiner contends that the crossbar switch was taught Morton and Potash was well known in the art to comprise horizontal and vertical conductors that were selectively connected via a grid or matrix or connection points. Morton taught the input and outputs to the cross bar switch were horizontal and vertical locations on the switch (e.g., see fig. 1) and the switch comprised plurality of for multiplexers that switched input and outputs (e.g., see col. 22, line 3- col. 23, line 7). Potash taught the inputs and outputs to the cross bar switch were at

horizontal and vertical locations on the switch (e.g., see fig.1). Potash taught multiplexers providing selection for "X" inputs and outputs and "Y" inputs and outputs for connection there between (e.g., see fig. 4). The Examiner contends this provides an equivalent to the conventional grid in cross bar switches with conductors at right angles to each other and using a selective connection at a grid point for connecting the orthogonal conductors. Consequently the Morton and Potash reference did teach a grid for transferring data between connected elements and since both taught connected ALUs or arithmetic units then they both comprised a grid connection between processing elements.

c) Morton and Potash do not teach transferring directly from a vector processor or ALU to a video buffer, or transferring from vector processor to the video buffer and from another vector processor to a memory interface in one cycle since there are multiple bus lines that can be defined by the programmer of the system. The Examiner contends that this is not claimed first of all. Further the system disclosed in the applicants figures does not provide for this connection for transfer directly from an ALU or video buffer or vector processor or to/form a video buffer. Since the figures in the instant application provide the ALUs connections parallel to each other (either both horizontal or both vertical) and memory at right angles then the connection would have provided connection of the ALUs to memory and not to each other. In order to connect ALUs to each other then more than one connection would have been required. The aspect of whether the transfer would have been performed in a single cycle comprised

how the system is controlled and the Examiner contends that there is nothing precluding the Morton and Potash systems from providing control for transfer in a single cycle.

d) Newly submitted and attached figure 1 is set up allegedly showing the configuration of the inventive processor with similar components as Morton. The figure 1 allegedly shows the output of the ALU can do directly to the memory via node switch 23 and the second ALU can allegedly connect to the video buffer via switch 32 and ALU is assumed to have an internal register to store the two data words to analyze. The Examiner contends that crossbar of Morton and Potash provides a means to directly connect the attached devices whether the devices are ALU or memory or something else. By merely locating the connected device a connectors at right angles to themselves then the transfer is readily performed in a single cycle. Even if Morton or Potash provided for timing adjustment between connected devices by sending the data to a buffer or cache before sending it to the destination device this still provides an invention that has the capablility of transfer in a single cycle by appropriate control signals to multiplexers in Potash or conversely the mere connection of the devices send/receive in a single cycle (with direct connection) placing them at right angles to each other connected to the crossbar switch. This would have been well within the skill of one of ordinary skill in the art. This direct connection is not claimed.

e) Newly submitted and attached figure 2 is the same as per Figure 1 except that the output of register B is fed into the input of register A, this allegedly shows the difference between the inventive system and Morton. Also the inventive system allegedly can perform multiple tasks in per clock cycle. Data allegedly cannot pass from

the instruction unit to buffered, video aware, DMA port without passing through the instruction cache. This allegedly shows the difference where the Morton processor allegedly needs to pass through other components to transfer data. There is allegedly only one data path for this operation whereas the inventive system allegedly can have multiple paths for the same operation. The applicant also alleges that newly submitted and attached figure 3 and figure 4 show plural switches where allegedly if one switch fails the system can bypass switches and still redirect the data through the switches to allow data to flow from ALU to memory interface or if an ALU failed data could be redirected to the other ALU so the other ALU could perform the computation of both ALUs. The Examiner contends that figures 2,3,4 newly submitted do not show configuration of a system as shown in the figures in the originally filed application. In the originally filed application the connection of ALUs and memory at connections at right angles. This is also the configuration in the Morton and Potash systems. As to providing plural paths the system in figure 4 of Potash provides plural outputs for the inputs that are selectively transferred depending on the output multiplexers and this provides for plural paths for direct connection this would provide for plural operations including transfers concurrently. The feature of bypassing failed switches is not claimed. Further the Morton and Potash system provide transfer of data to cache or registers as this provides timing adjustment for transfer to/from ALUs or processors. The system still provides connection for transfer of data between processors and other devices. Also the mere connecting of the ALUs or processors etc at orthogonal locations on the crossbar switch would have provided direct connection for transfer if a

delay for timing of transfers was not needed. This would have been within the level of skill of one of ordinary skill in the DP art.

f) Applicant alleges that the key difference between Morton and the instant claims is that the inventive system does not rely upon one component to share data and any processor element can connect to another processor element via a node switch where data does not have to pass through a data cache. And the inventive system can perform many PE to PE connections in one clock cycle and the number of PE connections depends upon the size of the processor and thus the grid size. Also the inventive system allegedly can be switched under program control and can have components with connect directly to another component via a node and the selection can be made by hardware or software. Morton and Potash taught a system that provides for connection between devices for sharing data as detailed in argument (E) above. As to the grid size Potash taught coupling the first crossbar to a secondary crossbar that connected other devices to each other (e.g., see fig. 1). As to the control being software or hardware interchanging of control in hardware or software was well known in the art at the time of the claimed invention and to Morton Potash taught a computer system (see outstanding rejection above).

g) Applicant alleges that the Potash patent has a limited bus size and limited number of buses where the inventive system a very large bus size and large number of buses depending on the number of node switches and the data in the Potash system must pass through the Scalar XBAR which has temporary memory for storing intermediate results and the inventive system does not require an intermediate stage as

allegedly shown in figure 1 of Potash, and the inventive system can directly transfer data directly from memory to an ALU and can output the result all in one clock cycle as as allegedly shown in figure 4 of the application. The Examiner contends that the Potash system has plural crossbar switches (scalar and vector) that connect devices for transfer of data (e.g., see fig. 1). This shows the concept of providing more than one crossbar switch for further expansion of the connections The features of an intermediate storage , direct transfer and one cycle transfer are discussed above.

h) Allegedly it would not have been a simple matter to combine the teaching of both patents to arrive at the present invention and there was no suggestion in Morton or Potash to make the combination and the patents allegedly do not teach the use of a grid with a plurality of node switches to interconnect the components of a computer system. The Examiner contends that it would have been obvious to combine the teachings of Morton and Potash as described above.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bolstad (patent No. 5,842,034) disclosed a two dimensional crossbar mesh for multi-processor interconnect (e.g., see abstract and figure 1).

Anderson (patent No. 4,331,956) disclosed a control means for a solid state crossbar switch (e.g., see abstract).

Gove (patent No. 5,696,913) disclosed a multiprocessing system with a switch matrix for connecting the processors (e.g., see abstract and fig. 4).

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (703) 305-9674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (703) 305-9712. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER